


Firmware Control sheet

	Drg	Gateway hex	
	Description		
Issue	ECN	Date	Reason for Change
1	n/a		First Issue

Device	18LF4620
R.F. Sols. ref.	

Design Requirements		
Feature	(Default)	Design / Customer Requirement
Ident. Mark	<i>Dot</i>	
Oscillator		INT RC, RA6, RA7 ports
Fail safe clock mon		Disabled
Oscillator Switch Enable		Disabled
Power Up Timer		Disabled
B.O.D.		Enabled in hardware
B.O.Voltage.		2.0V
Watchdog		Disabled,
Watchdog Postscaler		1:512
CCP2 Mux		RB3
Port B A/D Enable		Digital I/O on reset
Low power timer 1		Disabled
Master Clear Enable		MCLR Enabled
Stack Overflow Reset		Enabled
LV Program		Disabled
Code Protect		Disabled
Data EE Protect		Disabled
Read protect		All Disabled
Write protect		All Disabled
B'gnd. debug		Disabled

Serialisation?		No	
Type		Random	
Start Address		\$	
No of Words		decimal -	

Checksum	
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Other Requirements	If use of 16MHz crystal oscillator is required, set Oscillator configuration to HS.
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